REMARKS

This paper is being provided in response to the Office Action mailed March 10, 2004, for the above-referenced application. In this response, Applicant has amended claims 29-31 to clarify that which Applicant considers to be the invention. Applicant respectfully submits that the amendments to the claims are fully supported by the originally-filed specification.

Applicant thanks the Examiner for allowing claims 15 and 22-24. Applicant respectfully notes that in the Office Action dated September 2, 2003, the Examiner objected to claim 20 as apparently containing allowable subject matter but being dependent on a rejected base claim. Applicant subsequently rewrote claim 20 into independent form to incorporate the features of the base claim. Accordingly, Applicant respectfully submits that independent claim 20 is in condition for allowance.

The rejection of claim 19 under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement is hereby traversed. The Office Action indicates that the limitation "wherein when the logic signal is fixed at a low level during a standby state, one of said first capacitor and said second capacitor is set to an off-state in response to a chip select signal controlling said standby state, and the other of said first capacitor and said second capacitor is set to an off-state in response to said chip select signal that is negated" is seen as new matter because the specification as originally filed does not support this limitation. Applicant respectfully submits that this limitation is adequately supported and directs attention to, for example, Figure 9 and page 32, lines 2-4 of the present specification. Figure 9 shows n-MOS transistor N91 and p-MOS transistor P91, illustrated as capacitors, and which are respectively set

to off-states by the chip select signal CS and the negated signal /CS. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of claims 29-31 under 35 U.S.C. 112, second paragraph, as being indefinite is addressed by amendments contained herein in accordance with the comments set forth in the Office Action. Applicant has amended these claims to clarify that which Applicant considers to be the invention and for consistency with Applicant's remarks. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of claims 19-21, 27, 28 and 29-31 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,055,713 to Watanabe et al. (hereinafter "Watanabe") is hereby traversed and reconsideration is respectfully requested.

Applicant respectfully notes that claim 20 is currently independent, having previously been rewritten into independent form to incorporate the features of the base claim in response to a prior Office Action as noted above. Independent claim 20 does not appear to have been substantively addressed in the present Office Action, and Applicant respectfully submits that this claim is in condition for allowance.

Independent claim 19 recites a delay circuit. The circuit includes first and second nodes and first and second inverters. The first inverter receives a logic signal and its output is coupled to the first node. The input of the second inverter is coupled to the first node and the output is coupled to the second node. A first capacitor is coupled between the first node and a first power

source line, the first capacitor being a first transistor of a first channel type. The second capacitor is coupled between the second node and a second power source line different from the first power source line, the second capacitor being a second transistor of a second channel type different from the first channel type. Further, when the logic signal is fixed at a low level during a standby state, one of the first capacitor and the second capacitor is set to an off-state in response to a chip select signal controlling the standby state, and the other of the first capacitor and the second capacitor is set to an off-state in response to the chip select signal that is negated. Claim 21 depends on independent claim 19.

Independent claim 27 recites a delay circuit receiving a logic signal having a first logical level and a second logical level. An inverter chain is included including a plurality of inverters and at least one first capacitor, the inverter chain receiving a logic signal. The first capacitor includes a MOS transistor of a first channel type. The capacitor is operated to increase and decrease capacitance based on changes in the logical levels of the logic signal and whereby a first delay signal and a second delay signal are generated, the second delay time being shorter than the first delay time. A logical gate receives the output of the inverter chain and the logic signal so that the logical gate outputs its output signal in response to the first delay signal when the logic signal changes from the first logical level to the second logical level. Claim 28 depends on independent claim 27.

Independent claim 29, as amended herein, recites delay circuit. The circuit includes 2n+1 nodes defined in series, n being a natural number, a first node receiving a logical signal and 2n inverters, each inverter arranged between adjacent nodes of said 2n+1 nodes. A capacitor of an

n-MOS type is coupled between an even node and a power source line. A NOR gate is coupled to the first node and the (2n+1)th node.

Independent claim 30, as amended herein, recites a delay circuit. The circuit includes 2n+1 nodes defined in series, n being a natural number, a first node receiving a logical signal, and 2n inverters, each inverter arranged between adjacent nodes of said 2n+1 nodes. A capacitor of an n-MOS type is coupled between an odd node and a first power source line. A capacitor of a p-MOS type is coupled between an even node and a second power source line. An AND gate is coupled to the first node and the (2n+1)th node.

Independent claim 31, as amended herein, recites a delay circuit. The circuit includes 2n+1 nodes defined in series, n being a natural number, a first node receiving a logical signal, and 2n inverters, each inverter arranged between adjacent nodes of said 2n+1 nodes. A capacitor of an n-MOS type is coupled between an odd node and a first power source line. A capacitor of a p-MOS type is coupled between an even node and a second power source line. A NAND gate is coupled between the first node and the (2n+1)th node.

The Watanabe reference discloses an output circuit of an integrated circuit including first and second MOS transistors and a drive and control circuit. In Fig. 5, Watanabe discloses two inverters (I2 and I3), two capacitors (C1 and C2) and power source lines (VSS and VCC) with an output directed to a logic gate (a NAND gate-NA1); and in Figs. 7 and 11, Watanabe discloses the delay circuit with a NOR gate NG.

The Office Action indicates that no patentable weight has been given to the features previously added to independent claim 19 and restates the prior rejections over Watanabe. As noted above, Applicant has addressed the rejection of claim 19 under 35 U.S.C. 112, first paragraph, and respectfully submits that the cited feature is adequately supported by the specification as originally filed. Further, Applicant has amended claims 29-31, as noted above, to clarify that which Applicant considers to the invention. Accordingly, Applicant respectfully requests full consideration of claim 19 and resubmits the following remarks and arguments concerning the Watanbe reference with respect to Applicant's present claimed invention.

Applicant's independent claim 19 recites at least the features that when the logic signal is fixed at a low level during a standby state, one or more capacitors are set to an off-state in response to a chip select signal controlling the standby state. In structures based on MOS capacitors or inverters comprising MOS transistors, generation of leak current during the standby state is suppressed and thereby source-voltage dependency of the delay time is contained and power consumption is effectively controlled during the standby state. (See Figures 9, 10 and page 32, line 2 to page 33, line 4 of the present application.)

Applicant respectfully submits that Watanabe does not teach or fairly suggest at least the above-noted features as claimed by Applicant. Watanabe does not disclose the circuit configuration as claimed by Applicant including capacitors that comprise MOS transistors and wherein when the logic signal is fixed at a low level during a standby state, one or more capacitors are set to an off-state in response to a chip select signal controlling the standby state.

Accordingly, Applicant respectfully requests that the rejection of claim 19 be reconsidered and withdrawn.

Further, with respect to Applicant's independent claim 27, Fig. 5 of Watanabe discloses a delay circuit with a NAND gate NA1 and Figs. 7 and 11 of Watanabe disclose the delay circuit with a NOR gate NG. Regarding the inverted signal of signal C in Fig. 5, the rising edge is targeted for delay. On the rising of the inverted signal, the output signal of the inverter I2 falls and the output signal of the inverter I3 rises. Because the MOS capacitor C2 is supplied with the Vcc, it is a p-type MOS capacitor. Therefore, on the rising of the inverted signal, the MOS capacitors C1 and C2 are supplied with the signal so that their capacitance *decreases*. (See Figs. 5, 7 and 11 of Watanabe and timing diagrams showing delay in the Appendix attached to a previous response filed on June 10, 2003.)

In contrast, because the present invention makes a delay by *increasing* the capacitance, it differs from the delay circuit shown in Fig. 5 of Watanabe. The delay circuit shown in Figs. 7 and 11 of Watanabe also operates so that the capacitance of the capacitor in the delay circuit *decreases* when the level of the logic signal supplied to the delay circuit becomes the targeted level. Accordingly, in view of the above, Applicant respectfully requests that the rejection of claim 27 be reconsidered and withdrawn.

With respect to Applicant's claims 29-31, in Fig. 5 of Watanabe, the delay circuit with the NAND gate NA1 comprises three nodes and two inverters. The first node is supplied with the logical signal and the third node is connected to the NAND gate NA1. That is, the delay circuit shown in Fig. 5 of Watanabe comprises the inverter chain having (2n+1) nodes and 2n inverters.

The first node is supplied with the logical signal and the (2n+1)-th node is connected to the NAND gate NA1. In light of the above operations, an n-MOS capacitor is connected to *__an even node__* and a p-MOS capacitor is connected to *__an odd node__*.

In contrast, in the present invention, as shown in Fig. 6 of the present application, the delay circuit with NAND gate comprises the delay system D62. The delay system D62 comprises the inverter chain having (2n+1) nodes and 2n inverters. As indicated in Fig. 1A, the first node is supplied with the logical signal and the (2n+1)-th node is connected to the NAND gate. Moreover, in the present invention, an n-MOS capacitor is connected to *__an odd node__* and a p-MOS capacitor is connected to *__an even node__*. Therefore, the delay circuit with a NAND gate according to the present invention differs from the delay circuit shown in Fig. 5 of Watanabe.

Next, as indicated in Fig. 6 of the present application, the delay circuit with an AND gate according to the present invention comprises the delays system D61. The construction of the delay system D61 is the same as that of the delay system D62 (see Fig. 1A of the present application). Therefore, the delay circuit with the AND gate according to the present invention differs from the delay circuit shown in Fig. 5 of Watanabe.

Next, as indicated in Fig. 4 of the present application, the delay circuit with NOR gate according to the present invention comprises the inverter chain (2n+1) nodes and 2n inverters. The first node is supplied with the logical signal and the (2n+1)-th node is connected to the NOR gate. Moreover, in the present invention, an n-MOS capacitor is connected to *__an even node__*. In contrast, in the delay circuit with the NOR gate NG shown in Figs. 7 and 11 of Watanabe, an n-

MOS capacitor is connected to ***an odd node***. Therefore, the delay circuit with the NOR gate according to the present invention differs from the delay circuit shown in Watanabe.

Based on the above, Applicants respectfully request that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-248-4038.

Respectfully submitted,
CHOATE, HALL & STEWART

Date: August 17, 2004

Donald W. Muirhead
Registration No. 33,978

Customer No.: 26339
Choate, Hall & Stewart
Exchange Place
53 State Street
Boston, MA 02109
Phone: (617) 248-5000
Fax: (617) 248-4000